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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/708,642	
	Filing Date	03/17/2004	
	First Named Inventor	Chih-Chung Chuang	
	Art Unit	1765	
	Examiner Name	GEORGE, PATRICIA ANN	
Total Number of Pages in This Submission	47	Attorney Docket Number	ADTP0066USA

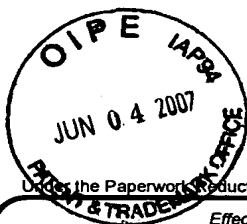
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Firm Name	North America Intellectual Property Corporation
Signature	<i>Winston Hsu</i>
Printed name	Winston Hsu
Date	05/30/2007
Reg. No.	41,526

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FEE TRANSMITTAL For FY 2007

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$) 0.00

Complete if Known

Application Number	10/708,642
Filing Date	03/17/2004
First Named Inventor	Chih-Chung Chuang
Examiner Name	GEORGE, PATRICIA ANN
Art Unit	1765
Attorney Docket No.	ADTP0066USA

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description

Each claim over 20 (including Reissues)

Fee (\$)
Small Entity Fee (\$)

50 25

Each independent claim over 3 (including Reissues)

200 100

Multiple dependent claims

360 180

Total Claims Extra Claims Fee (\$)

Fee Paid (\$)

- 20 or HP = x =

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims Extra Claims Fee (\$)

Fee Paid (\$)

- 3 or HP = x =

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets Extra Sheets Number of each additional 50 or fraction thereof Fee (\$)

Fee Paid (\$)

- 100 = / 50 = (round up to a whole number) x =

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Fees Paid (\$)

Other (e.g., late filing surcharge):

SUBMITTED BY

Signature	<i>Winston Hsu</i>	Registration No. (Attorney/Agent)	41,526	Telephone	3027291562
Name (Print/Type)	Winston Hsu	Date	05/30/2007		

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Electronic Acknowledgement Receipt

EFS ID:	1815022
Application Number:	10708642
International Application Number:	
Confirmation Number:	2641
Title of Invention:	METHOD FOR FABRICATING LIQUID CRYSTAL DISPLAY PANEL ARRAY
First Named Inventor/Applicant Name:	Chih-Chung Chuang
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	ADTP0066USA
Receipt Date:	30-MAY-2007
Filing Date:	17-MAR-2004
Time Stamp:	04:27:00
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 500
RAM confirmation Number	12180
Deposit Account	503105
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Appeal Brief Filed	ADTP0066USA0_A8_1.pdf	914344	no	11

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2	Fee Worksheet (PTO-06)	fee-info.pdf	8175	no	2
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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Electronic Patent Application Fee Transmittal

Application Number:	10708642			
Filing Date:	17-Mar-2004			
Title of Invention:	METHOD FOR FABRICATING LIQUID CRYSTAL DISPLAY PANEL ARRAY			
First Named Inventor/Applicant Name:	Chih-Chung Chuang			
Filer:	Winston Hsu			
Attorney Docket Number:	ADTP0066USA			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Filing a brief in support of an appeal	1402	1	500	500
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				500



Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Patent Application of)
)
Chih-Chung Chuang,) Group Art Unit: 1765
Shin-Jien Kuo,)
Chao-Yun Cheng,) Examiner: GEORGE, PATRICIA ANN
Shu-Feng Wu)
) Appeal No.
Application No.: 10/708,642)
) Attorney's Docket No. ADTP0066USA
Filed: March 17, 2004)
)
For: METHOD FOR FABRICATING)
LIQUID CRYSTAL DISPLAY PANEL
ARRAY

BRIEF FOR APPELLANT

Assistant Commissioner for Patents

10 Washington, D.C. 20231

Sir:

This appeal is from the decision of the Examiner dated 03/09/2007, finally rejecting claims 1-12, which are reproduced as an Appendix to this brief.

15 The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 50-3105. This paper is submitted in triplicate.

INTRODUCTION

A. Real Party in Interest

The present application is assigned to AU Optronics Corp.

B. Related Appeals and Interferences

The legal representative and assignee do not know of any other appeals or interferences which will affect or be directly affected by or have bearing on the Board's decision in the pending appeal.

C. Status of Claims

Responsive to the first Official Action in this application, on November 16, 2005, an Amendment was filed to amend claims 1, 3, 7, 14, 16 and 20 in response to the Examiner's objections, 35 U.S.C. 112, second paragraph and 35 U.S.C. 103 (a) rejections set forth in the first Official Action.

Responsive to the first final Official Action in this application on April 13, 2006, an Amendment was filed canceling claim 16 without prejudice and amending claim 13 in response to the Examiner's objections, 35 U.S.C. 102 (e) rejections set forth in the first final Official Action.

Responsive to the second Official Action in this application on January 4, 2007, an Amendment was filed amending claim 1 in response to the Examiner's objections, 35 U.S.C. 103 (a) rejections set forth in the second Official Action. Hence, claims 1-15 and 17-20 are currently pending in this application.

Responsive to the second final Official Action in this application on May 28, 2007, an Amendment was filed canceling claim 6 in response to the Examiner's objections, 37 C.F.R. 1.75 (c) rejections set forth in the second final Official Action and amending claim 3. Hence, claims 1-5, 7-15 and 17-20 are currently pending in this application.

Pursuant to 37 C.F.R. §1.191(a), applicant hereby appeals the Examiner's decision finally rejecting claims 1-5 and 7-12 to the Board of Patent Appeals and Interferences.

D. Status of Amendments

A second Official Action was issued on 08/17/2006 rejecting claims 1-12 under 35 U.S.C. §103(a). In response to the second Official Action, applicant filed a response and an amendment arguing that the application is patentable over the cited references. The subsequently issued second final Official Action dated 03/09/2007,
5 indicated claims 1-12 being rejected.

A copy of the claims at issue on appeal is attached as Appendix A.

SUMMARY OF THE INVENTION¹

The primary object of the present invention is to provide an improved method
10 for fabricating liquid crystal display devices, thereby alleviating or eliminating Mura defects of LCD panels.

Another object of the present invention is to provide a method for forming a Mo/AlNd, MoW/AlNd, or MoW/Al dual-layer metal array of LCD panels by using
15 End-Point Detection (EPD) instead of prior art time-mode etching.

The preferred embodiment of the present invention includes the steps of providing a substrate having a main surface; depositing a dual-metal layer such as Mo/AlNd, MoW/AlNd, or MoW/Al onto the main surface of the substrate; defining
20 gate and word line patterns using layers of photoresists; and using the photoresists as an etching mask, a first metal dry etching process is carried out to etch the dual-metal layer at an etching selectivity that is significantly higher than prior art. The first metal dry etching process uses oxygen/fluorine containing an etching gas mixture and oxygen/chlorine containing an etching gas mixture to form the dual-metal gate and
25 word line patterns having slightly oblique sidewalls. End point detection mode is used in the first metal dry etching process.

¹ This summary is provided in accordance with 37 C.F.R. §1.192(5) and Section 1206 of the Manual of Patent Examining and Procedure, and is not intended to limit the subject matter of the claimed invention to the specific embodiment described herein.

The present invention is emphasized on the improvement of uniformly etching of the upper metal of the dual-metal layer. Further, the etching selectivity between the upper metal and the lower metal of the dual-metal layer is increased such that more reliable end-point detection in the first metal dry etching process can be used. In addition, to avoid so-called white pad effects, the ashing rate of the photoresist is reduced due to recipe change.

THE REJECTIONS, REFERENCES AND EXAMINER'S POSITION

A. The Rejections

10 Claims 1, 6 and 7 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. (USPN 6429057) in view of Rioux (USPN 5554488) and Kim et al. (4981816).

 Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. (USPN 6429057) and Rioux (USPN 5554488) in view of Kim et al. (4981816) and Przybysz et al. (USPN 4904980).

 Claims 3, 9, 10, 11 and 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. (USPN 6429057), Rioux (USPN 5554488) and Kim et al. (4981816) in view of Hori et al. (USPN 5445710).

20 Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. (USPN 6429057) Rioux (USPN 5554488) and Kim et al. (4981816) in view of Cheung et al. (USPN 5354417).

 Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. (USPN 6429057) Rioux (USPN 5554488) and Kim et al. (4981816) in view of Celii et al. (USAN 10/282,621).

25 Claim 8 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hong et al. (USPN 6429057) Rioux (USPN 5554488) and Kim et al. (4981816) in view of Nagata et al. (JP405067590A).

B. The References

30 i. Hong et al. (USPN 6429057)

Hong et al. discloses a front end array process for making an LCD panel (col. 1.7-11), comprising: depositing a molybdenum-containing metal gate layer which consists of gate line, gate pads, and gate electrodes that can have a single or multiple layered structure and is deposited on a silicon substrate. Hong teaches the use of photolithography masking followed by dry etch to pattern the molybdenum-containing metal layer for forming both gate and data wire, but Hong fails to teach substantially oblique sidewalls.

ii. Rioux (USPN 5554488)

Rioux discloses a method of forming a semiconductor structure. The method provides for a gate structure comprising a multilayer metal stack characterized by smoothly tapered sidewalls (i.e. the resulting gate structure 54, as shown in FIG. 10), with substantially no undercut in which the taper angle may be controlled. The tapered gate structure 54A comes from the second conductive layer 48 deposited over the tungsten silicide layer 46 (FIG. 7). The discontinuity 50 over the sidewall propagates into the tungsten layer 48.

iii. Kim et al. (4981816)

Kim et al. teaches a metal for fabricating contact structure through via opening in VLSI circuits employs a dual layer of refractory metal. First a thin titanium layer is deposited, over which a molybdenum layer is formed. An annealing treatment further improves contact resistance characteristics. A preferred etch resolution is achieved using RIE of molybdenum, etched until gas is cut off at the detection of the molybdenum end point.

C. The Examiner's Position

The Examiner's apparent position with respect to the rejections based on 35 U.S.C. §103(a), is that Rioux discloses a conventional method of forming Mo containing metal gate with tapered sidewalls, i.e. oblique sidewalls, formed on the surface of a semiconductor substrate through use of well known photolithography and dry etching method as recited in claim 1. The Examiner recognizes that Hong fails to teach substantially oblique sidewalls. The Examiner has attempted to remedy this

deficiency by attempting to combine the tapered sidewalls disclosed in Rioux reference with Hong et al. (USPN 6429057).

IV. ISSUES

5 The issue on appeal is whether claim 1 is properly rejected under 35 U.S.C. §103(a) as being unpatentable over over Hong et al. (USPN 6429057) in view of Rioux (USPN 5554488). This issue is discussed below under Section V.

V. ARGUMENT

10 **The Rejection of Claims 1 Under 35 U.S.C. §103(a) is Improper**

 Independent claim 1 defines a front-end array process for making a liquid crystal display panel. The method includes depositing a molybdenum-containing metal layer on a glass substrate, wherein said molybdenum-containing metal layer is a dual-metal layer; forming a patterned photoresist on said molybdenum-containing
15 metal layer, wherein said patterned photoresist defines a gate and word line array pattern; and using said patterned photoresist as an etching mask, uniformly **etching** said molybdenum-containing metal layer to form said gate and word line array pattern having substantially oblique sidewalls ... In other words, the **substantially oblique sidewalls** is the direct result of the uniformly etching of the
20 molybdenum-containing metal layer.

 The Examiner attempts to combine the method disclosed in Hong et al. (USPN 6429057) in view of the smoothly tapered sidewalls of Rioux (USPN 5554488) and Kim et al. to achieve the claimed invention.

25 -----

2143.03 All Claim Limitations Must Be Taught or Suggested

 To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ
30 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35

U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

5

i. Improper Combination

The Examiner alleges that Hong et al. discloses a front end array process for making the LCD panel (col. 1.7-11), comprising: depositing a molybdenum-containing metal gate layer which consists of gate line, gate pads, and gate electrodes that can have a single or multiple layered structure and is deposited on a silicon substrate. Hong teaches the use of photolithography masking followed by a dry etch to pattern the molybdenum-containing metal layer for forming both gate and data wire, but fails to teach substantially oblique sidewalls. The Examiner relies on the smoothly tapered sidewalls of Rioux to overcome this deficiency. However, the applicants point out that the profile of the smoothly tapered sidewalls of Rioux is not formed by etching but by deposition.

The smoothly tapered sidewalls of Rioux are first shown in FIG. 7. A second conductive layer 48 comprising tungsten is deposited over the tungsten silicide layer 46 (FIG. 7). Simultaneously, the tapered discontinuity 50 over the sidewall propagates into the tungsten layer 48, which establishes the tapered profile. In other words, the deposition of the conductive layer 48 is the essential reason for the formation of the tapered gate structure 54.

The Examiner asserts that "Rioux discloses a conventional method of forming Mo containing metal gate with tapered sidewalls, i.e. oblique sidewalls, formed on the surface of a semiconductor substrate through use of well known photolithography and dry etching method." (emphasis added) Applicants disagree with this assertion. Given the above, as a matter of fact the **deposition** of the conductive layer 48 is the **essential reason of the formation of the tapered gate structure 54, NOT by the so-called "well known photolithography and dry etching."** It appears that the Examiner is attempting to use non-analogous art and incorrect combination reasoning in attempting to achieve the claimed invention.

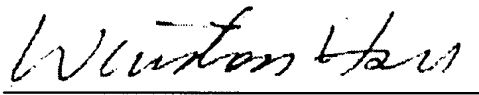
In the light of the above reasons and lack of disclosure of every feature, the applicants firmly believe that these distinct features distinguish the present invention from the combination of cited prior art references. To sum up, claims 1 is patentable over Hong et al. (US 6,429,057) in view of Rioux (US 5,554,488) and Kim et al.

5 Furthermore, as claims 2-5 and 7-12 are dependent upon claim 1, they are in the condition for allowance

VI. CONCLUSION

10 For at least the reasons set forth above, it is respectfully submitted that the rejection of claims 1-5 and 7-12 are improper and should be reversed.
Respectfully submitted,

15 Sincerely yours,



Date: 05/30/2007

Winston Hsu, Patent Agent No. 41,526

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in
25 D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

APPENDIX

The Appealed Claims

5

1. (Previously presented) A front-end array process for making a liquid crystal display panel, comprising:

depositing a molybdenum-containing metal layer on a glass substrate, wherein said molybdenum-containing metal layer is a dual-metal layer;

10 forming a patterned photoresist on said molybdenum-containing metal layer, wherein said patterned photoresist defines a gate and word line array pattern; and

using said patterned photoresist as an etching mask, uniformly etching said molybdenum-containing metal layer to form said gate and word line array pattern having substantially oblique sidewalls, wherein said etching of said

15 molybdenum-containing metal layer uses gas mixture, wherein said etching of said molybdenum-containing metal layer is detected by an end-point detection method.

2. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein after said etching of said molybdenum-containing metal

20 layer, an over etching is carried out.

3. (Previously presented) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said gas mixture is SF₆/O₂ having a ratio of about 700sccm/300sccm.

25

4. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said etching of said molybdenum-containing metal layer is executed under a process pressure higher than 25 mTorr.

30 5. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said etching of said molybdenum-containing metal layer is further controlled by a source power, a bias power, process pressure, oxygen

flowrate and flowrate of fluorine containing gas.

6. (Canceled)

5 7. (Previously presented) The front-end array process for making a liquid crystal display panel according to claim 6 wherein said dual-metal layer is Mo/AlNd, MoW/AlNd, or MoW/Al, wherein Mo and MoW are top layers, while AlNd and Al are bottom layers.

10 8. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said etching of said molybdenum-containing metal layer is detected by an end-point detection method at an wavelength of about 704nm.

15 9. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said gas mixture is oxygen/fluorine containing.

10. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said gas mixture is oxygen/chlorine containing.

20 11. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said gas mixture is oxygen/chlorine/fluorine containing.

12. (Original) The front-end array process for making a liquid crystal display panel according to claim 1 wherein said gas mixture is SiF₆/O₂ containing.

25

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